"Power Electronic Building Block Design and Hardware Demonstrator - Results From December 1996 Through May 1998"

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Abstract

The Power Electronic Building Block (PEBB) program, sponsored by the Office of Naval Research, seeks to develop a general purpose power module capable of performing numerous electrical power conversion functions simply through software reconfiguration. This program is broken into 3 stages. Stage 1 covers PEBB function. Stage 2 covers PEBB form and function. Stage 3 covers PEBB form, fit and function. This paper reports on the Naval Surface Warfare Center Annapolis Detachment efforts in Stage 2 - PEBB form and function. The concept of a PEBB is independent of topology. A soft switched power conversion topology was desired to maximize system efficiency for the NSWC PEBB. Using a combination of MCTs (MOS Controlled Thyristors) and IGBTs (Insulated Gate Bipolar Transistors) manufactured by Harris Semiconductor the auxiliary resonant commutated pole (ARCP) PEBB was developed to test emerging semiconductor devices, namely the p-type and n-type MOS-Controlled Thyristors (MCT). Power semiconductors and circuit phase leg design changes and control enhancements relative to the PEBB-1 functional demonstrator will be discussed. Waveform data from PEBB 1.5 will be presented and discussed.

Background

This work was funded by the Office of Naval Research under the Power Electronic Building Block Program. The goal of the PEBB program is to enable the application of more electric power conversion for US Navy ships through the affordable implementation of advanced electrical power conversion techniques and components. NSWC was tasked to investigate the use of soft switching inverter

technology in a multifunctional electrical power converter. Concurrently, ONR tasked Harris Semiconductor to team with NSWC to produce the core building blocks comprising the converter.

The chosen power converter circuit topology was the Auxiliary Resonant Commutated Pole (ARCP) zero voltage switching inverter. The Navy had previously worked with GECR&D on the ARCP as a candidate for DC-AC ship service inverter module (SSIM) application under the Navy's Integrated Power System (IPS) Program. NSWC used the GE design as its starting point using core elements produced by Harris Semiconductor. It should be noted that the core elements produced by Harris were specifically tailored to an ARCP circuit topology based upon guidance provided by NSWC. Although these particular devices were tailored to the ARCP, the process employed in their manufacture and the Harris ThinPak™ die could be cost effectively utilized in virtually all circuit topologies.

PEBB1 Core Devices

PEBB1 core devices supplied by Harris (Figure1) included half bridge power modules, AC Switch modules, gate drives and a water-cooled heat sink. The half bridge module acted as the ARCP main switching elements. It originally incorporated p-type MOS controlled Thyristors as the power semiconductor. Later versions were supplied with non punch-through Insulated Gate Bipolar Transistors. Additionally, n-type MCT based modules were supplied to another Navy program in a beta-site agreement with the PEBB program. The AC modules employed p-type MCT's as the bi-directional switching elements.

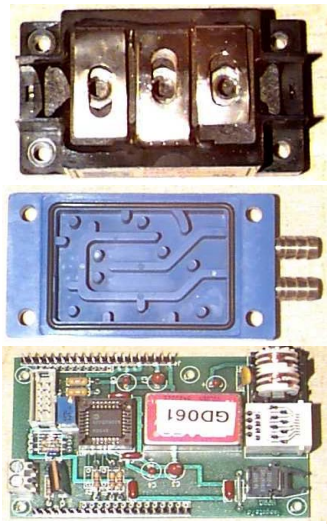

Figure 1 - PEBB1 Core Devices

Both the half bridge and AC switch modules were designed to have a very low thermal resistance to the cooling fluid employed. The backside of the ceramic substrate holding the semiconductor die was exposed at the base of the module. The water cooled heat sink attached to the bottom of the module to provide direct water cooling of the back of the ceramic. The tradeoff with this approach was the loss of thermal capacitance achieved with a traditional heavy copper baseplate.

The gate drives supplied provided universal drive power for p-type and n-type MCT's as well as IGBT's. It also included a jumper selectable zero voltage turn-on mode to accommodate the ARCP requirement of a soft turn-on of a main switch.

PEBB1.5 Core Devices

As a result of lessons learned from the PEBB1 core devices, modifications were made which resulted in the PEBB1.5 core devices (Figure 2 and 3). The first lesson learned was that the p-type MCT's presently capable of being manufactured by Harris have a turn-off current tail which is significantly longer than an equivalently rated IGBT. This prevented its practical application as an ARCP main switch. However, its extremely high di/dt turn-on and peak current withstand ratings are much higher than an equivalent IGBT, making it an ideal ARCP auxiliary or AC switch. As a result, PEBB1.5 main switch modules presently employ non-punch-through IGBTs, whereas the PEBB1.5 AC switch module employs a

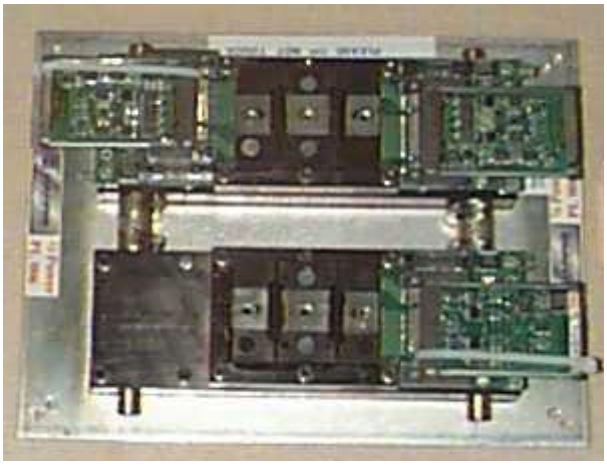

Figure 2 - PEBB1.5 Core Devices

combination of n-type and p-type MCTs. This combination of n and p-type devices allows the use of gate drive circuits that can be referenced to the relatively stable midpoint of the DC bus, minimizing the risk of false triggering due to noisy gate returns. Because of the high current withstand rating of the MCT's employed in the AC switch module, it was possible to include a thick film snubber resistor inside the module. Since the resistor was mounted to the water-cooled ceramic substrate, it was a much smaller alternative to what was needed in the PEBB1 design.

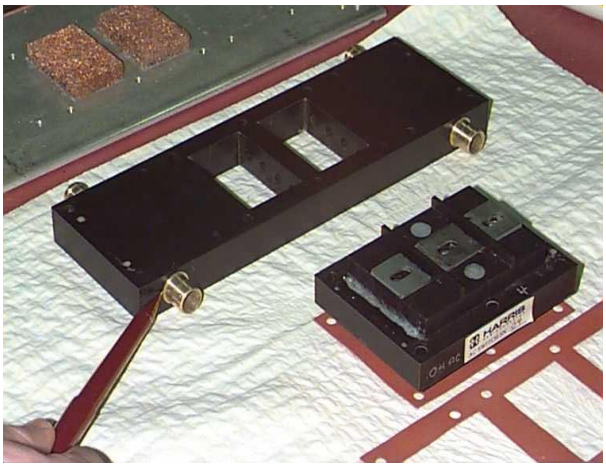

Figure 3 - PEBB1.5 Disassembled

The other area of improvement was the addition of water-cooled copper sponges directly bonded to the ceramic baseplate of the module. These sponges were then encased in a plastic assembly, which allowed better water flow than the PEBB1 design. The heatsink improvements allowed the safe dissipation of 1kW per switch module for the PEBB1.5 design versus 400W per module for the PEBB1 design.

Perceived Benefits of ARCP

The ARCP inverter is perceived to have the following beneficial features in comparison to a hard switched inverter:

- Lower Loss
- Higher Efficiency
- Lower Device Stress
- Lower High Frequency EMI
- Friendlier to the load in terms of dV/dt and dI/dt

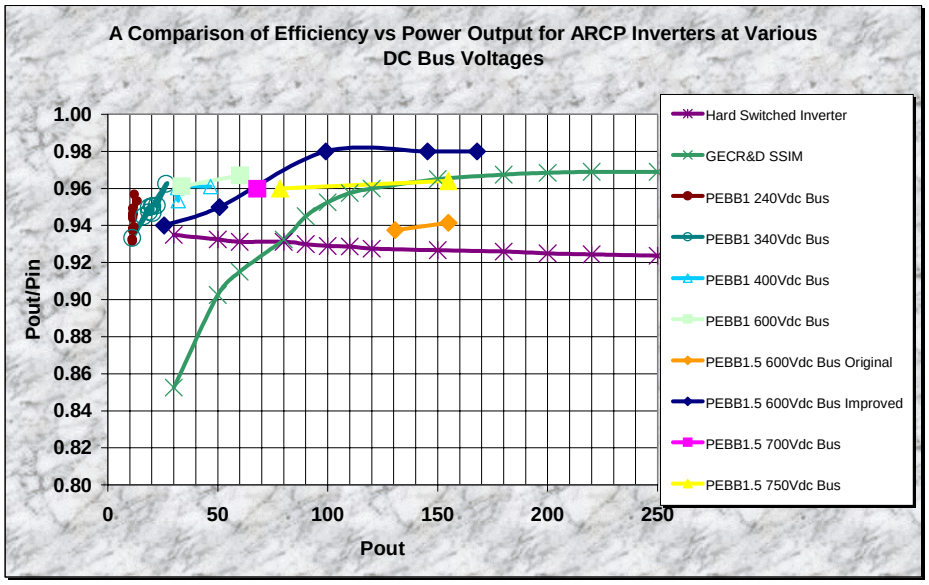

Figure 4 Efficiency vs. Output Power

A low power ARCP inverter was designed, built and tested by PSU under an NSWC PEBB contract to investigate high frequency converter issues. It employed IGBT Main switches and FET auxiliary switches. As an ARCP operating at 190VDC input, 14A output, the inverter was able to operate up to a 63.4 kHz switching frequency. The same hardware was then operated as a hard switched inverter at the same input voltage and load current. The maximum operating switching frequency attained was 32.5kHz at which point switching losses in the main devices were excessive enough to fail the device. This experiment seemed to verify that the ARCP did indeed have lower losses[1].

Experiments were performed by GECR&D and NSWC on ARCP inverters, comparing their efficiencies to those of a typical hard switched inverter. The results are summarized in Figure 4. The conclusion is

that at or near rated load current, the ARCP does operate more efficiently than a hard switched inverter. However, as the inverter is operated at lower percentages of rated load, the fixed amount of losses produced by the non-ideal resonant components in the ARCP become more apparent and eventually make the ARCP less efficient. The break even point between a hard switched and ARCP inverter varies for the 3 units shown in the figure. This variation is attributable to differences in power switching devices employed, switching frequency, and control algorithm employed. The solution seems to be to develop a circuit which could operate as an ARCP above some power level and operate as a hard switched inverter below the break even point. [2]

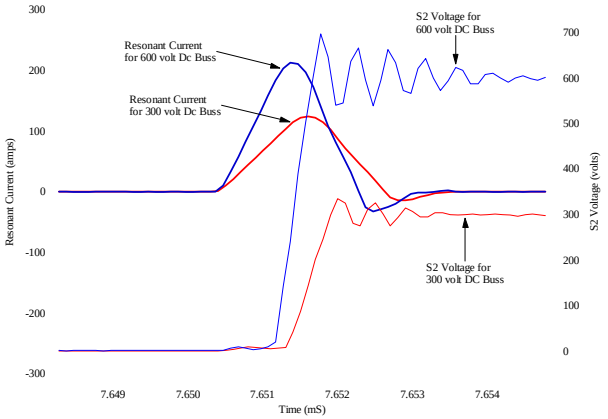

Figure 5. ARCP Resonant Transitions.

The last three points in the list -Lower Device Stress, Lower High Frequency EMI, Friendlier to the load in terms of dV/dt and dI/dt, are all attributable to the Zero voltage turn-on and controlled dv/dt turn-off of the main switches, inherent in the ARCP inverter. Figure 5 shows a typical ARCP switch transition. Peak voltage overshoots are less than 20%.

Perceived Tradeoffs

The consequence of going to an ARCP inverter are perceived as:

- Higher parts count
- Higher cost

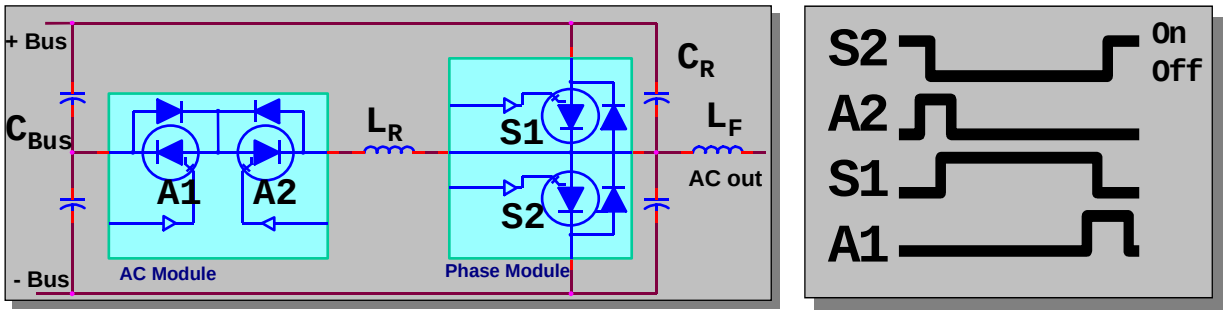

Figure 6. ARCP schematic and switch timing.

Higher Parts Count

Figure 6 shows a single phase version of an ARCP inverter showing the primary elements. A hard switched converter would not need the AC switch, the resonant inductor or the resonant capacitors, however, a snubber circuit may be required in place of the resonant capacitors. Starting from the DC bus and working toward the output, we will discuss what is required from each of the parts. The DC bus capacitors supply high frequency ripple demanded by the PWM switching scheme employed by both an ARCP and a hard switched inverter. The hard switch demand may be worse than soft switch due to the shape of the demanded voltage waveform - square wave vs. trapezoidal. For an ARCP, the DC bus caps must also supply resonant current pulses every switching cycle. The net DC bus cap requirements for

both a hard switched inverter and an ARCP probably end up being about the same.

Three parts present in an ARCP, but not found in a hard switched inverter are the AC switch, the resonant inductor and the resonant capacitors. The devices in the AC switch must be rated for half the DC bus voltage and, although the peak resonant currents approach 800A at high power, the pulses are of extremely short duration and the devices turn off at zero current. In fact, the RMS value of the resonant current required for 250kW operation is approximately 50A. The resonant inductor sees the same current as the AC switch and must be sized accordingly. Since the resonant current contains high frequency components, the inductor was manufactured using Litz wire. The relatively low inductance value of 1 to 1.5 microhenries made the inductor somewhat difficult to manufacture accurately. This became important because the controller needed to know precisely how much time to leave the AC switch turned on in order to insure zero-voltage turn-on of the phase switch. Too little resonant current would produce a hard switch transition. Too much would resonant current would put unnecessary current stresses on the AC and main switches, producing higher losses and lower efficiency. The solution was to measure the inductance, matching the three inductors as closely as possible for a three phase inverter, and programming the actual value into the controller.

The last of the resonant components – the resonant capacitors, are sized based on the tail current of the main switch device. It was important to have an accurate capacitance value with little or no temperature drift throughout its operating cycle. Because of this requirement, NPO dielectric capacitors were employed, which are presently expensive. Unless a comparable hard switched inverter employs snubber components, these resonant capacitors put the ARCP at a disadvantage here.

Parts count may also be an issue in the areas of feedback control signals, sensors and analog I/O. In addition to monitoring output voltage for regulation purposes, the present NSWC ARCP implementation monitors input DC bus and output load current to provide the information needed for proper resonant switch transitions. The DC input bus voltage measurement requirement is low bandwidth, but reasonably high accuracy. The Output load current measurement requirement is both high bandwidth and high accuracy.

Higher Cost

Given the fact that the above parts count discussion points toward the ARCP having more parts, one can conclude that this would in turn lead to higher cost. Given the present commercial practices employed in power conversion equipment manufacture, this would be correct. However, the goal of the PEBB program is to develop an automated manufacturing process using pick and place assembly techniques to produce modules employing the proper types of semiconductor switches, diodes and ultimately passive and control components interconnected in the circuit topology requested by the circuit designer.

Harris PEBB1.5 modules employing HTP™ semiconductor die in a generic, user definable arrangement begin to demonstrate a way of removing the costly hand assembly process from power converter manufacturing. In addition, a significant amount of effort was made in order to minimize the cost and size impact of the additional components required for the ARCP to operate. The key was to supply the minimum amount of resonant energy to allow a zero voltage transition to occur. This would minimize the current handling requirements of the additional components needed, thereby minimizing the additional cost burden.

Auxiliary Resonant Pulse Control

The central reason for the selection of the ARCP topology for the NSWC PEBB was the exact reason it was not selected by others. The ARCP requires resonant devices to have current ratings that exceed the main switch requirements and have a very high di/dt capability. Because the auxiliary switch only sees this stress for a short period of time the ideal solution would be a fully controllable switch with high

di/dt withstand and a surge rating that would allow a small device with respect to the main switch to meet the requirements. The MCT fits this requirement exactly.

It appears that the higher the di/dt within the auxiliary resonant circuit, the better. During an ARCP cycle, time spent transitioning the output node to the opposite rail is time lost from the available duty cycle. (Of course, there is a direct correlation between the maximum realized duty cycle and the ratio of input to output voltage which relates back to overall converter efficiency.) So for maximum output voltage, maximum di/dt is desirable. However, there are additional issues to consider. During an ARCP cycle when transitioning from a main switch to the opposite diode within a phase leg, the device is required to turn off both the instantaneous load current and the boost current. Contributing to this issue is the controllability of the resonant currents when a large di/dt exists. Excessive resonant di/dt will result in imprecise boost control, which dictates overboosting and a loss of efficiency and main switch current margin. As part of an efficient design, a balance must be found between enough boost energy, and main switch current turn off ratings, and between auxiliary current controllability and maximum realizable duty cycle. The case just discussed is special for an ARCP, when the load current and the resonant current is additive within a switch, the direction of the load current assists in the rail to rail transition. This however, does not mitigate the concerns of requiring the main device to have additional turn-off capacity. When the load current alone is sufficient to swing the output node to the opposite rail, no boost is required. The auxiliary boost pulses are not required and can be inhibited. However, when the load is not sufficient the auxiliary resonant circuit can augment the load current with a reduced resonant contribution (reduced with respect to energy that would be required under a no load condition). This modification tapers the resonant current pulses significantly prior to reaching the point of auxiliary pulse inhibit. Work is on-going in this area to determine what the optimum resonant current modulation should look like.

The present NSWC ARCP uses a Load Modulated Auxiliary Resonant Current (LMARC) control strategy which is a practical application of the theoretical ARCP control described in Reference [3]. This approach was developed in stages, to minimize the risk to the hardware. The goal of the LMARC software was to provide the minimum amount of resonant energy to the circuit to allow a zero voltage transition to occur. This in turn produces the least amount of current stress to the main and auxiliary switches and improves overall inverter efficiency. LMARC works by feeding back the instantaneous three phase load currents to the ARCP controller. The current information is critical since the direction indicates whether the load current is assisting (“Load Assist”) or inhibiting (“Diode Displacement”) the removal of charge from the resonant capacitors. The magnitude of the current is used to calculate the resonant current required to commutate the diode (“Diode Displacement”) or to reduce the required boost energy during “Load assist”. The initial implementation of this control algorithm maintained a fixed auxiliary to main switch overlap time for all switching events. As mentioned previously, this reduced the load current capability of the main device. LMARC modulates the auxiliary current pulses during “Diode Displacement” so that the auxiliary current at the instant prior to resonance is equal to the load plus a fixed boost current. For the “Load Assist” condition at the instant of resonance the auxiliary current is reduced proportional to the magnitude of the load current. When the boost energy is reduced to the minimum, the auxiliary current pulses are completely inhibited and the load alone displaces the resonant capacitor charge and swings the output node to the opposite rail. This is significant since the auxiliary current modulation during “Load Assist” is the transition that initially required more turn-off capability of the main device. In an efficiently designed ARCP the load current alone should transition the output to the opposite rail at a current level low enough such that the maximum current turn-off stress of the main device is the peak of the load current. Therefore, no additional current rating of the main devices is required. This is true in the NSWC ARCP inverter.

To illustrate these concepts a few examples may be helpful. At light load the resonant pulses are approximately equal in magnitude, alternating in positive and negative directions identical to fixed auxiliary current operation (See Figure 7). When load current increases, resonant current pulses begin to modulate in magnitude based on the instantaneous load current. Increasing where switch transitions were made from a conducting diode and decreasing when transitioning from a conducting switch. Figure 8 shows the waveforms captured during the initial implementation of the LMARC control program. As can bee seen in this diagram there is a phase shift between the envelope of resonant pulses and the actual load current. This is due to the phase lag between output current measurements, calculations and auxiliary resonant current implementation. Improvements were made to the software reducing the sampling to implementation delay from 840 to 120 degrees of the switching period (One switching period equals 360 degrees.). Figure 9 shows how this improvement affected the waveforms by aligning the envelope of resonant pulses more closely with the load current. A further enhancement within the LMARC control program was to eliminate unneeded resonant pulses or to perform auxiliary current pulse inhibit. As can be seen in Figure 10, the resonant pulses are eliminated when the load current is above 90 amperes. At this point the highest current turn off is either the sum of the auxiliary current and instantaneous load current at the point of pulse inhibit, or the peak load current. For our implementation the maximum main switch currents were the former case.

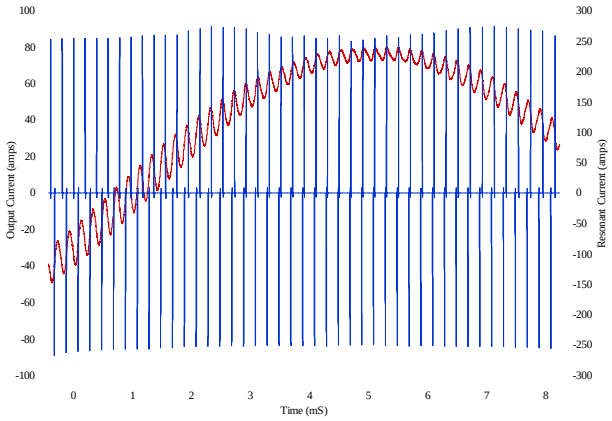

Figure 7. Fixed overlap time.

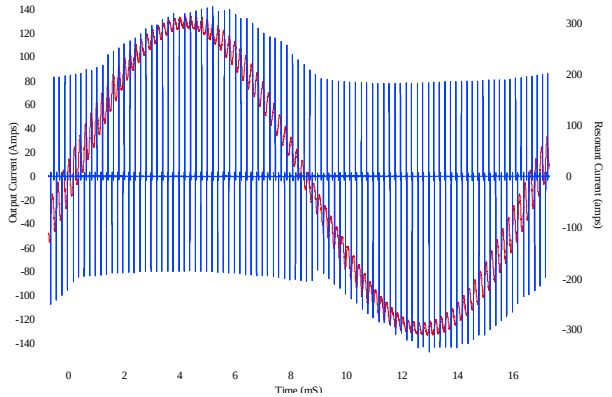

Figure 8. Load Modulated Auxiliary Resonant Current (LMARC) Control.

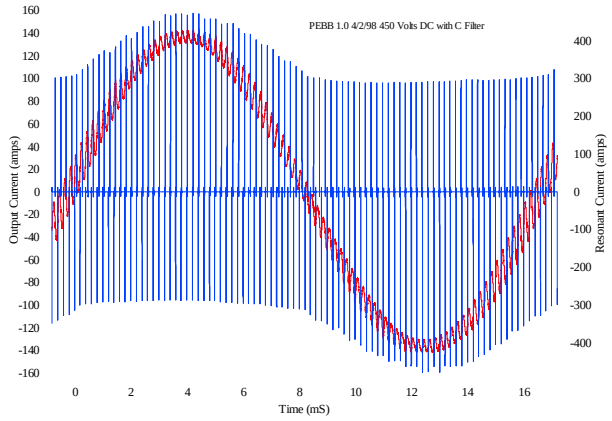

Figure 9. Improved LMARC

As covered earlier, further reduction in resonant current losses and a reduction of the main device turn off requirement was achieved by an inverse modulation of the auxiliary current based on instantaneous load current. This modification tapers the resonant current pulses to nearly zero prior to reaching pulse inhibit (See Figure 11). Consequently the maximum main switch turn-off requirements for the NSWC ARCP occur at the peaks of the load current. With a full implementation of LMARC, it is projected that approximately 50A rms of resonant current will be required for a full 250kW (330A rms) of output load.

Maximum Duty Cycle Limitation

Utilizing state space averaging[4], the idealized line-to-line RMS voltage obtainable from a three phase PWM ARCP inverter is given by:

$$V_{L-L,RMS} = \frac{\sqrt{3} * m_a * V_D}{2 * \sqrt{2}} * (2 * duty_{\max} - 1)$$

$$V_{L-L,RMS} \cong 0.612 * m_a * V_D * (2 * duty_{\max} - 1)$$

Where m_a is the amplitude modulation ratio and V_D is the DC bus voltage [5]. A common drawback of soft switching inverter topologies is the amount of time needed to perform the resonant switch cycle. This reduces the amount of duty cycle time available to synthesize the output waveform. Typically, for a hard switched inverter, one allows a few microseconds of "dead time" between the turning off of an upper switch and the turning on of a lower phase switch and vice versa during the other transition. This is done to prevent a shoot through condition from occurring where both an upper and lower device are on simultaneously, shorting out the DC bus. This limits maximum duty cycle values to approximately 95-97%. In addition to the "dead time" found in hard switched inverters, soft switched inverters add resonant transition times which can push this maximum duty cycle value down significantly. An analysis of soft switching schemes reveals that some topologies fare better than others when it comes to how much time is lost due to resonant transitions. One of the reasons the ARCP inverter was chosen over other topologies was that its transition cycles were on the lower side of the spectrum compared to others [6]. Nevertheless, the NSWC ARCP had to deal with the trade off of maximizing DC bus utilization while producing high quality output waveforms through the use of high switching frequencies. At 5kHz switching frequency, the NSWC ARCP was able to operate at a maximum duty cycle of 90%. This represents a loss of 20 microseconds, which is completely unacceptable to achieve our next goal of 250kW at 20kHz. To obtain the same voltage gain at 20kHz that we presently have at 5kHz, the maximum duty cycle must be maintained at 90%. In other words the total time lost from the maximum achievable duty cycle must shrink from 20 to 5 microseconds.

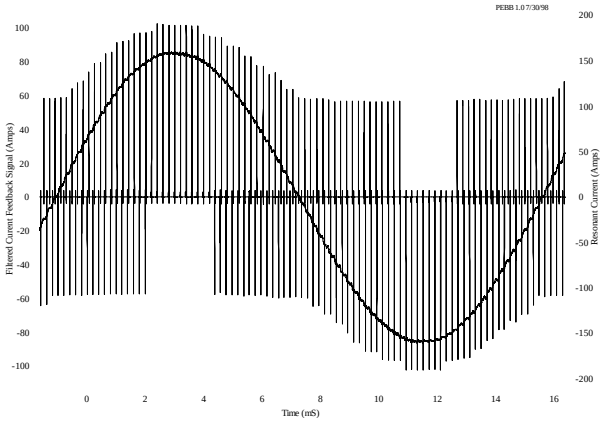

Figure 10. Pulse Inhibit

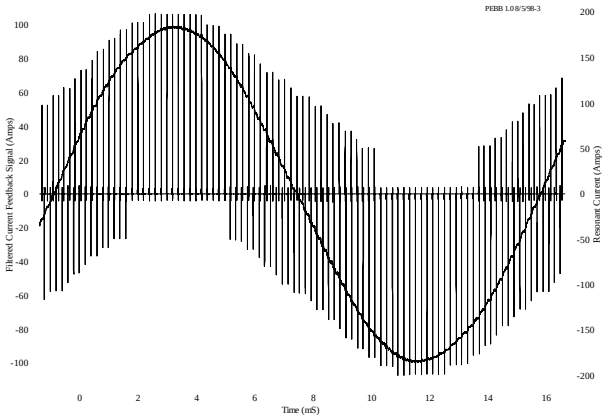

Figure 11. Modified Pulse Inhibit

In fairness, the existing control strategy loses 13.5 microseconds, we have kept additional 6.5 microseconds as a margin for safety. Of the 13.5 microseconds, more than half is due to the limitations of our control implementation. Current work is transitioning to a new controller and a new control implementation to achieve the maximum possible ARCP duty cycle at a reduced cost.

Voltage Balance

Improvements in the control software have also been made with respect to three-phase output voltage balance. Initial test runs had always yielded several volts of unbalance between the three phases. (See the low voltage comparison data in Table1.) The software was modified to compensate for two con-

tributing factors. The duty cycle is indirectly controlled in the present NSWC ARCP realization. Originally there was an implicit assumption that the difference between the two auxiliary resonant inductor charge times within the switching cycle was negligible. This is not in fact the case. Second, the software was modified to compensate for the $1/3^{rd}$ of a switching cycle between phases.

Phase A-B Voltage (Vac)	Phase B-C Voltage (Vac)	Phase C-A Voltage (Vac)	Phase Voltage Unbalance % (Worst case dev. /average)	Control Algorithm
137.4	134.4	137.4	1.47	Without Voltage Balance
136.6	136.4	136.6	0.10	With Voltage Balance

Table 1. Voltage Balance Before and After Software Implementation.

Third Harmonic Voltage Injection

In order to get maximum output voltage from a given input voltage, the control algorithm was modified to include the technique known as third harmonic voltage injection. See references [4] and [7] for an explanation of how this works. The net result of incorporating this into the control algorithm was a 15% increase in phase to phase voltage over the original algorithm.

Additional Issues uncovered during analysis and testing

As one works to remove cost from one part of a converter, other parts begin to drive up the cost. This was evident in the output filter employed. One of the fundamental reasons for going to a soft switching converter such as an ARCP is to push the switching frequency as high as possible in order to separate the fundamental output frequencies the load wants from the harmonic frequencies generated by the PWM switching algorithm. At higher switching frequencies smaller L and C values are required to filter the harmonics from the output. Unfortunately, at the voltage and current levels required for electrical power distribution, there seems to be some difficulty in locating inexpensive, compact, high frequency, high power inductors.

A second issue is that dropping out of ARCP due to insufficient boost or failure of a main switch to latch the output node to the appropriate rail, can result in the auxiliary switch supplying the load current. At the end of the predetermined auxiliary switch cycle the device will turn off. This stresses the auxiliary switch because it has a minimal snubber designed only for the reverse recovery of the auxiliary diode. Under moderate to high load currents this can result in a catastrophic failure.

Conclusion

The NSWC PEBB as presently implemented as an ARCP inverter has been demonstrated at 200kW.

Refinements are continuing, which allow the ARCP to achieve higher performance and multiple power conversion functions.

The areas where improvements can be made are:

- A method of partitioning ARCP-specific control circuitry as close to the phase leg as possible in order to allow traditional controllers to be employed

- An automated module assembly process that would allow the ARCP to be easily manufactured with minimal hand assembly
- Less expensive high performance capacitors and inductors

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